An Automated Electrical Defect Identification and Location Method for CMOS Processes Using a Specially Designed Test Chip

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***Abstract*—A test chip (Yieldchip) was designed, simulated, fabricated and tested on a 3 micron process. The layout of the Yieldchip's cells enable the test program to electrically locate and identify active faults, thereby automating the classification of defects. The Yieldchip can detect more than one defect per circuit in most circumstances. The algorithm can identify the 21 simple defects of the cells and can be used as an expert system to extend this list. Unidentified detectable faults are flagged at all times and located if possible.**

Objectives

TO IMPROVE and model process yields, a test vehicle is needed to perform defect recognition. Defects are induced by processing and they cause electrical faults through interaction with the design. The CMOS test vehicle we designed [named Yieldchip] is to be processed as a standard device and was designed to enable automatic electrical defect identification and location [1].

Test chips have been used in the semiconductor industry since its early years. They have evolved with time in complexity and subtlety. The Yieldchip is a dedicated test chip, its function being to help the engineer locate and identify defects induced by processing.

We believe that this test chip represents a major breakthrough in defect identification, as the defects can be identified with the test program using electrical measurement data.

Traditionally, structures like the serpentine/comb [2], [3] and RAM arrays [4], [5] have been used as tools for yield improvement work. The serpentine/comb structures are perfectly good for single layer problem solving, although they cannot be used on all layers (well implants for example). Their use for yield monitoring is also limited by the large area they require.

On the other hand, the RAM arrays are very good for locating defects, but defect type identification is tedious and can only be done visually in some cases. In the RAM arrays the electrical signature of the fault does not easily lead to the physical nature of the fault. The peripheral circuitry is also prone to defects, but this is usually only a slight inconvenience.

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Devising a method to locate and identify faults has been attempted by some workers before [5], [6], and [7]. Stapper [5] was one of the first to recognize the difference between defects and faults. He had considerable success using this difference to model the yield of DRAM. Buehler [6] designed a test chip in which the transfer characteristics of simple CMOS inverters can be measured. This enabled him to locate defective inverters. This circuit requires one transmission gate per inverter for the electrical isolation of the inverter's output, therefore, it is prone to faults on the transmission gates.

Newhart [7] described lately a test chip which performs automated defect location. This circuit consists of a rather complicated array of NMOS or PMOS transistors. Newhart claims that this test chip can identify all faults through unique electrical patterns. Unfortunately his paper does not explicitly show this.

We developed the Yieldchip to combine the best of the two basic structures used for yield monitoring: to electrically locate faults (as with RAM arrays) and identify faults (as with serpentine/comb) through unique signatures (the term patterns was used in [7]). This paper describes the design of the Yieldchip and the principles behind its conception.

Approach

Electrically speaking, the effect (signature) of a fault is dependent upon two things: its location and its nature. Both of these factors affect the signature of the fault. If the section of the chip where the fault happened is repetitive, then the signature on the faulty cell will be similar, no matter on which cell the fault occurred. Only resistive effects can make a difference in this case.

The localization of the fault can be fairly easily achieved, the use of an array of some sort will most likely be adequate. But, the identification of the fault is not so obvious. To perform the identification we rely on voltage values at the output of each base cell row for different digital input signals. The set of the analog values read for each cell is called a signature.

To decrease the probability that different physical faults give the same electrical signature, some principles help: simple design, geometric orthogonality for conductive layers, complementary devices, and analog design. Sim-

plicity is probably the most important one; the more complex the cell is, the more chances there are of having the same signature for different faults.

One extreme example of this is that of a VLSI wafer on which are found functional and non-functional circuits. The signature of the defect can be taken as the functionality or the non functionality of each circuit. Obviously, it is impossible to tell what is the electrical fault simply by receiving the information "functional" or "nonfunctional", because the circuit is too complex.

To use geometric orthogonality helps to reduce possible redundancy of the signatures, and often makes the design simpler. The main device of the cell should be transistors since this is the main active component of integrated circuits.

Design

The design principles listed above can be achieved with an array of transmission gates (Fig. 1). The array is expanded by mirroring the original cell in the X and the Y direction. This enables neighboring cells to share the same P-well, making the electrical path to ground less resistive, thus improving grounding. This is especially important for large test chips where the P-well may be more than a few millimeters long and could otherwise pose substrate biasing problems on the n-type transistors.

The cells are connected as follows: all drains/sources of one row are connected together with metal; all P-channel/N-channel gates of one column are connected together with polysilicon. Polysilicon routing in one direction and metal in the other introduce orthogonality of the conductive layers in the array and reduce chances of signature redundancy.

Minimum design rules are used everywhere in the main array to increase the sensitivity to defects. The P+ diffusion grounding stripe in the transmission gate array is an exception to this rule and is made larger to improve grounding.

The basic idea of the Yieldchip is to turn on one column of transmission gates and then to apply digital 0 or 1 to a row of transmission gates sources and to read the analog voltage at the drain row. This way, the functionality of each cell is tested.

In order to be able to sense the voltage at each drain row of the transmission gates, the drain lines are fed into an analog demultiplexer (Fig. 2). To reduce external components and improve speed, the output of the analog demultiplexer includes a linear voltage compressor (20% Vdd to 80% Vdd) and an analog buffer.

This additional circuitry takes little silicon and is very useful. Compression of the signal is required before the buffer because its output cannot fully swing to both supplies. The voltage compressor is made of a three resistor T-network (equivalent resistance of 1 MΩ).

Three D-latch arrays are used to supply the column decode, row address, and output demultiplexing signals. To save pad area the D-latch arrays share a common data input and a common reset input. Eleven pads are required for all the connections. The last bit of each D-latch array is used to verify functionality. This is an important feature. It ensures that the transmission gate array is being addressed and read properly.

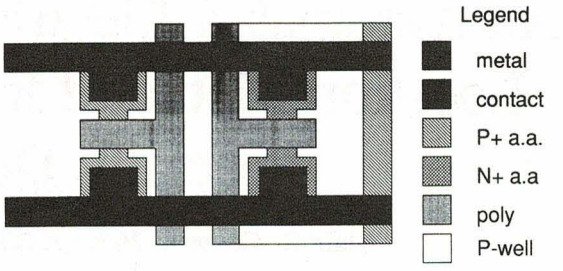

Fig. 1. Physical layout of the transmission gate cell. Expansion of the array is done by mirror reflection in X and Y directions.

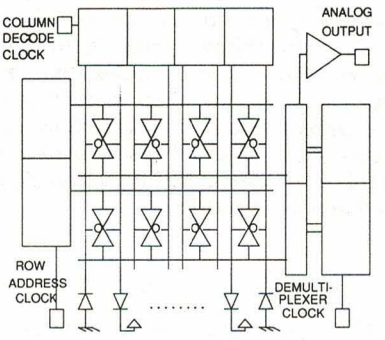

Fig. 2. Simplified building blocks of the Yieldchip. The array size shown here is limited to 4 × 2 for clarity.

The input of the analog buffer is connected to the data input pad when the D-latch arrays are in the reset mode. This enables verification of the buffer and the voltage compressor by the test program.

To ensure that a voltage is present on the gates in case of a break in a polysilicon line, the unused end of the column decode polysilicon lines are biased to a fixed potential through reverse-biased diodes. The potential used is such that the transistors connected to the line are in the "ON" state if the other end of the polysilicon line is disconnected.

Four digital combinations are used to encode the source inputs of each row (Table I). For that purpose the source inputs are divided in two groups: the source input of the selected row; and the sources of the rest of the array. These two groups enable 4 combinations of digital 0 and 1 (00, 01, 10, 11) to be applied sequentially to the transmission gates sources. The data read at the analog output of the selected row (drain) is used to form a 4 bit word, each bit corresponding to one of the 4 combinations applied to the sources.

Tri-level bit values are used to encode the output v. These are defined as follows for Vdd = 5 V: in high impedance (no column selected) $0 = (v < 1.90)$, $1 = (v > 3.00)$, and $X = (1.90 < v < 3.00)$; in normal mode $0 = (v < 1.20)$, $1 = (v > 3.75)$, and $X = (1.20 < v < 3.75)$.

TABLE I
THE DIFFERENT COMBINATIONS USED TO ENCODE THE SOURCES OF THE TRANSMISSION GATE ARRAY (ACCORDING TO THIS TABLE, THE OUTPUT IN NORMAL MODE AT THE DRAIN IS 0011 IF THERE IS NO DEFECT)

	Combinations			
	00	01	10	11
Cells above	0	1	0	1
Selected cell	0	0	1	1
Cells below	0	1	0	1

Other combinations of source bit encoding can be used. It is quite possible that such different bit patterns may help to reduce some remaining redundancy, but at the moment of writing this paper we have found the 4 combinations shown in Table I to be satisfactory.

In normal mode, only one column is selected at any given time. Each cell is sensed by addressing its column and selecting its drain output. The array is also read in high impedance mode. In this case, each reading gives information on all the cells within the row, and not on any specific cell. Used in conjunction with the normal mode, the high impedance mode helps to differentiate defects which have similar signatures in normal mode.

The size of the transmission gate array has some importance. If the array is excessively large, the probability that the peripheral circuitry will not work on each die increases unacceptably. Therefore not enough die with working peripheral circuitry would be present per wafer. On the other hand, if the array size is too small, the peripheral circuitry will be disproportionately large compared to the transmission gate array size. In this case, the total number of cells sensed per wafer would be reduced because the peripheral circuitry uses too much silicon. In addition, most defects would be on the peripheral circuitry.

The number of cells probed per wafer (N) is used to estimate the best size for the array. N is the number of cells on die for which the peripheral circuitry is functional. The number of cells probed is proportional to the total number of cells per wafer ($N_{\text{cell/wafer}}$) (1) and to the yield of the peripheral circuitry (2):

$$N_{\text{cell/wafer}} = N_{\text{die/wafer}} \times N_{\text{cell/die}} \tag{1}$$

$$N = N_{\text{cell/wafer}} e^{-D*Ap} \tag{2}$$

Ap is the area of the peripheral circuitry. The use of the pessimistic Poisson yield model is adequate for our purpose. Fig. 3 shows the number of cells probed as a function of the defect density (D) for different array size. An increase in array size corresponds to an increase in the potential number of cells sensed, while the effect of the defect density is to impose a limitation on the size through its effect on the peripheral circuitry. In our case the size of the transmission gate array is currently 128 × 256. This proves to be a good choice for defect densities below 10 def./in^{-2}.

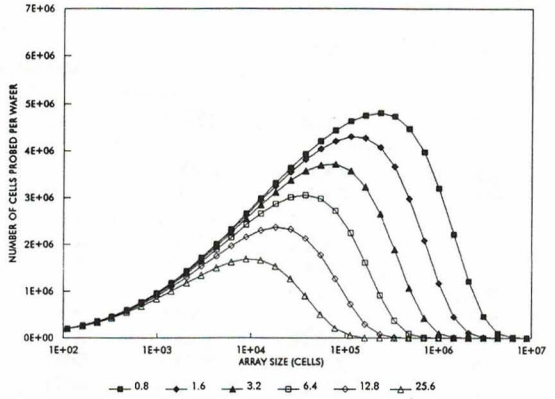

Fig. 3. The number of cells probed on 100 mm wafer as a function of the transmission gate array size and defect densities per square inch (using Mitel's 3 μm design rules).

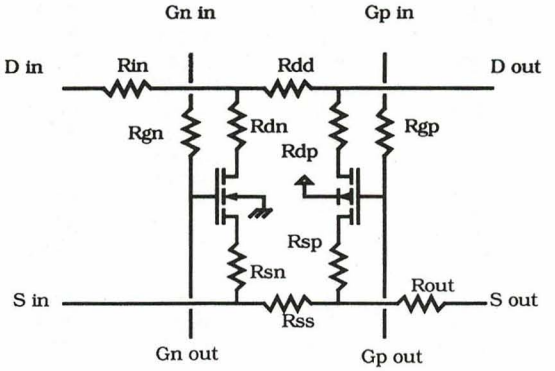

Fig. 4. The equivalent circuit of the transmission gate cell used for the simulations. No defects are shown here.

RESULTS

An analog simulator (HSPICE) was used to simulate the electrical defects and find their signatures. For that purpose a 16 × 16 array was used. The equivalent circuit used for the transmission gate cell is shown in Fig. 4.

Only the faults which affect internal nodes of the cell and external nodes between neighboring cells are considered. To obtain the list of the possible shorts within the cell, we neglect all the resistances and we look for all the combinations of the remaining nodes. This reduces the number of combinations without affecting the physical interpretation of the faults, because the resistances involved have very small values (metal or contact).

The open conductor or open contact faults are determined by each resistor which may be absent. The 21 resulting faults are listed in Table II. Only 2 faults cannot be differentiated: open drain, and open source. This is not very important anyway because sources and drains are interchangeable.

We defined a set of mnemonics to name the faults. The convention we used is the following: G, D, S are the transistor terminals, B is the transistor substrate, O means an open at one terminal; the last character is the transistor type (N or P). If the letter O is absent then it is a short between the two nodes.

TABLE II
DEFECTS SIGNATURES LISTED WITH MNEMONICS AND RELEVANT COMMENTS. TWO SETS OF SIGNATURES ARE IDENTICAL FOR HIGH RESISTANCE SHORTS (DBN GDN AND DBP GDP)

Type	*Hi-Z*	*YHi-Y*	*Left*	*Local*	*Right*	*Ydir*	*XY*	Comments
$S_nS_{n-1}O$	XXXX	XXXX	0011	XXXX	XXXX	0011	XY	
SSO	XXXX	XXXX	0011	XX11	XXXX	0011	XY	Even column
	XXXX	XXXX	0011	00XX	XXXX	0011	XY	Odd column
DDO	XXXX	XXXX	XXXX	00XX	0011	0011	XY	Even column
	XXXX	XXXX	XXXX	XX11	0011	0011	XY	Odd column
$D_nD_{n-1}O$	XXXX	XXXX	XXXX	XXXX	0011	0011	XY	
SBN	XXXX	XXXX	00XX	00XX	00XX	0011	Y	Rmax 200K
SBP	XXXX	XXXX	XX11	XX11	XX11	0011	Y	Rmax 100K
GBN	XXXX	XXXX	0011	XX11	0011	XX11	XY	Rmax 100K
GBP	XXXX	XXXX	0011	00XX	0011	00XX	XY	Rmax 100K
DON	XXXX	XXXX	0011	XX11	0011	0011	XY	
DOP	XXXX	XXXX	0011	00XX	0011	0011	XY	
GSN	XXXX	X0XX	00XX	XX11	00XX	X011	XY	Rdef 1K–5K
	XXXX	X0XX	00XX	XX11	00XX	0011	XY	5K–100K
GSP	XXXX	XX1X	XX11	00XX	XX11	001X	XY	Rdef 1K–5K
	XXXX	XX1X	XX11	00XX	XX11	0011	XY	5K–100K
DBN	0000	XXXX	00XX	00XX	00XX	0011	Y	Rmax 200K
	0000	XXXX	0011	0011	0011	0011	Y	200K–5M
DBP	1111	XXXX	XX11	XX11	XX11	0011	Y	Rmax 100K
	1111	XXXX	0011	0011	0011	0011	Y	100K–5M
GDN	0000	XXXX	00XX	XX11	00XX	0011	XY	Rmax 100K
	0000	XXXX	0011	0011	0011	0011	Y	100K–5M
GDP	1111	XXXX	XX11	00XX	XX11	0011	XY	Rmax 100K
	1111	XXXX	0011	0011	0011	0011	Y	100K–5M
GG	0011	0011	0011	0011	0011	0011	Y	Up to 10K
DS	0011	XXXX	0011	0011	0011	0011	Y	Rmax 8M
S_nD_{n-1}	0101	XXXX	0XX1	0XX1	0XX1	0XX1	Y	100–1K
	0101	XXXX	0011	0011	0011	0011	Y	1K–1M
GON	XX11	XX11	0011	0011	0011	0011	Y	
GOP	00XX	00XX	0011	0011	0011	0011	Y	

For example GDN is a short between the gate and the drain of the N-channel device; DS is a short between the drain an the source of a cell; and DDO is an open between N-channel and P-channel drain.

When the fault occurs between two neighboring cells, the subscripts n, $n-1$ or $n+1$ are added to the corresponding cells terminals. For example: $S_nS_{n+1}O$ is an open between the sources of two neighboring cells.

Simulations were done for each fault. Only the case where there is one fault per array was simulated. The signatures of each fault (Fig. 5) include output words defined as: *Hi-Z, YHi-Z, Local, Right, Left* and *Ydir. Hi-Z* is the word read at the faulty row in high impedance. *YHi-Z* are the words read on rows below the faulty row in high impedance. *Local* is the word read at the faulty cell in normal mode. *Left* are the words read to the left of the faulty cell. *Right* are the words read to the right of the faulty cell. *Ydir* are the words read below the faulty cell. Any of the words read on neighboring cells that give an affected signature (not 0011) is called a shadow.

The simulations indicate that the words left, right and below the defective cell are always identical to the nearest neighbor words left, right and below the cell. This greatly reduces the information set required to identify the fault.

Table II lists the defect signatures for low resistance shorts and the X-Y identification capability. Some signatures change when shorts have a higher resistance, but this typically occurs for resistances above 1 MegaOhm.

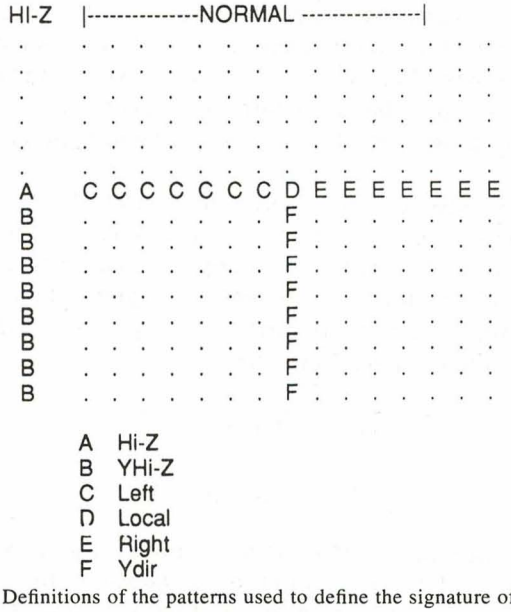

Fig. 5. Definitions of the patterns used to define the signature of the fault.

In some cases this causes signatures to become identical for different faults.

From the simulation results, it appears that if two faults are present the only case where they can not be identified is when their signatures overlap. If one fault projects a shadow (F in Fig. 5) in the Y direction (*YHi-Z, Ydir*) and the other fault projects a shadow in the X direction (*Hi-Z,*

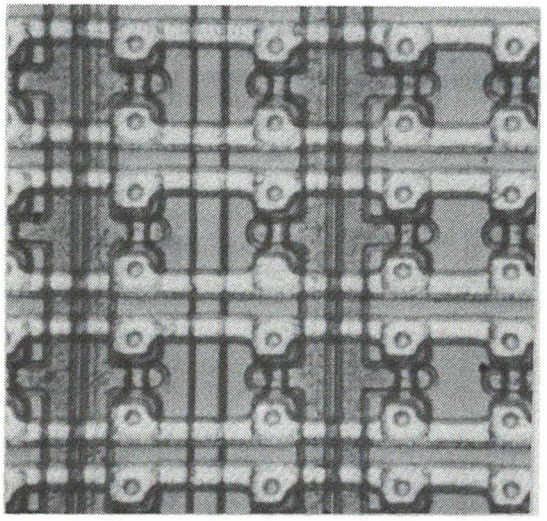

Fig. 6. Missing contact identified and located with the yieldship. The defect found was an open drain on the N-channel device (DON).

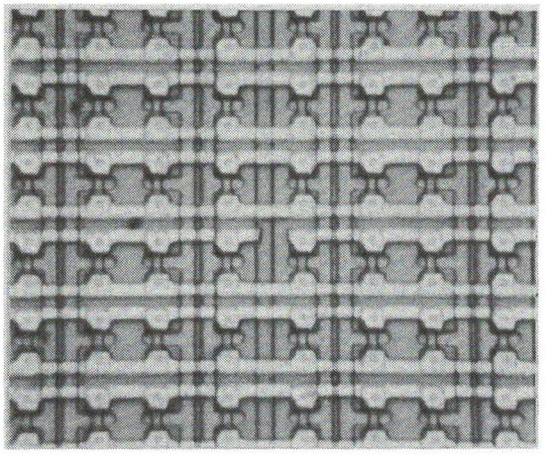

Fig. 7. An open metal line identified and located with the Yieldchip. The defect found was a open between the sources of neighboring cells ($S_n S_{n-1} O$).

Left, Right), the intersection of the two shadows may be interpreted by the algorithm as the defect location.

The simulations also show that all faults can be identified. The X-Y location of the faults is possible in about half of the cases. It is interesting to note that if the fault can be identified electrically, then it is not important to be able to locate it except to verify its physical nature or the algorithm.

The test program is written to recognize the signatures, but first, it must verify the functionality of the peripheral circuitry. If the circuit passes this initial test, the array is first read in high impedance state (no column selected). The array is read row by row beginning with the cell opposite to the column decode D-latch and close to the row decode D-latch (bottom right corner in Fig. 2). In normal mode, each column is sequentially selected within a row and the analog output is read for each of the 4 combinations of source encoding applied to that row. This is then repeated for all rows.

The test is done with a PC interfaced to a semi-automatic prober. The test program was written in *C* language, testing of each circuit takes about 15 seconds. The classification used for defect signatures opens the door to system expertise in the test program. It is easy to add new signatures to the program if there is a need for it.

The circuit was fabricated with a 3-micron single metal and single polysilicon process. Electrical tests showed the Yieldchip works as predicted by the simulations; it enables electrical identification and location of process induced faults in the array. Figs. 6 and 7 show some defects which were located and identified electrically with this tool. At this point, the physical nature of a fault cannot be assigned to a signature in all cases. As yet, the set of possible physical defects for each electrical fault is greatly reduced. Description of this set is not complete yet, and is beyond the scope of this paper.

However, some of the results obtained from two lots are included in Tables III and IV. Sample size is not the same for both tables (defect counts should be weighted by the total number of defects for each sample), and good

TABLE III

ELECTRICAL SIGNATURE VERSUS PHYSICAL DEFECT TYPE CLASSIFICATION FOR LOT 10433 (ROW LABELED 'UNKNOWN' INDICATES A DEFECT THAT COULD NOT BE LOCATED EVEN THOUGH IT MIGHT HAVE AN IDENTIFIABLE SIGNATURE. COLUMN LABELED 'UNKNOWN' INDICATES A DEFECT WITH AN UNIDENTIFIABLE SIGNATURE ALTHOUGH IT MIGHT HAVE BEEN POSSIBLE TO LOCATE. DEFECTS GROUPED IN THE DOTTED BOXES ARE DISCUSSED IN THE TEXT)

	TOTAL	DsN	DsP	GDN	GDP	GG	DS	SnDn-1	GON	GOP	SnSn-10	SSO	DDO	DnDn-10	SsN	SsP	GsN	GsP	DON	DOP	DONP	GSN	GSP	Unk.
Physical defect																								
Type 1:	31	0	1	0	0	0	0	7	0	0	0	1	0	0	0	0	0	0	12	1	1	0	0	8
Type 2:	39	0	0	0	0	1	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	33
Type 3:	6	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	3
Type 4:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Type 5:	35	0	0	0	0	29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	5
Type 6:	59	1	2	4	5	6	2	0	0	2	0	4	1	0	0	0	0	0	0	1	0	2	3	26
Type 7:	6	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4
Type 8:	14	0	3	0	0	4	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	6
Type 9:	46	0	0	0	0	14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	32
Type 10:	10	0	0	0	0	0	0	3	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	6
Type 11:	14	10	0	0	0	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0	0
Type 12:	88	0	25	0	0	0	0	0	0	0	0	0	1	0	0	35	0	0	0	1	0	0	0	26
Type 13:	136	0	11	0	0	0	0	0	0	0	0	0	0	0	0	76	0	0	0	0	0	0	0	5
Type 14:	87	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	33	35	4	0	0	15
Type 15:	41	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	20	20	1	0	0	0
Type 16	33	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	21	8	0	0	0	5
Type 17:	16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16	0	0	0	0	0
Type 18:	35	0	0	0	0	0	2	9	0	0	1	4	4	0	0	0	0	0	0	1	0	0	0	14
Type 19:	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2
Type 20:	15	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	13
Type 21:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Unknown:	220	1	0	2	0	19	21	24	0	3	1	2	0	0	0	0	0	0	0	0	0	2	0	145
TOTAL	933	12	86	7	5	74	25	49	0	5	2	12	6	1	5	112	0	0	102	67	6	5	5	347

TABLE IV

ELECTRICAL SIGNATURE VERSUS PHYSICAL DEFECT TYPE CLASSIFICATION FOR LOT 11851 (ROW LABELED 'UNKNOWN' INDICATES A DEFECT THAT COULD NOT BE LOCATED EVEN THOUGH IT MIGHT HAVE AN IDENTIFIABLE SIGNATURE. COLUMN LABELED 'UNKNOWN' INDICATES A DEFECT WITH AN UNIDENTIFIABLE SIGNATURE ALTHOUGH IT MIGHT HAVE BEEN POSSIBLE TO LOCATE. DEFECTS GROUPED IN THE DOTTED BOXES ARE DISCUSSED IN THE TEXT)

	TOTAL	DsN	DsP	GDN	GDP	GG.	DS	SnDn-1	GON	GOP	SnSn-10	SSO	DDO	DnDn-10	SsN	SsP	GsN	GsP	DON	DOP	DONP	GSN	GSP	Unk.
Physical defect																								
Type 1:	109	0	0	0	0	0	7	75	0	0	0	0	0	0	0	0	0	0	11	2	0	0	0	14
Type 2:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type 3:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Type 4:	19	0	0	0	0	0	0	6	0	0	0	0	0	0	0	0	0	0	0	13	0	0	0	0
Type 5:	2	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Type 6:	202	1	4	12	13	67	6	4	1	3	0	0	0	5	1	0	1	0	3	3	0	6	5	67
Type 7:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type 8:	5	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	3
Type 9:	122	0	0	0	0	0	36	0	34	27	0	0	0	0	0	0	0	0	13	0	0	0	0	12
Type 10:	15	0	0	0	0	0	0	0	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0	11
Type 11:	15	6	0	0	0	0	0	0	0	0	0	0	0	0	9	0	0	0	0	0	0	0	0	0
Type 12:	221	0	83	0	0	0	0	0	0	0	0	0	0	0	0	121	0	0	0	1	0	0	0	16
Type 13:	96	0	36	0	0	0	0	0	0	0	0	0	0	0	0	59	0	0	0	0	0	0	0	1
Type 14:	25	0	0	0	0	1	0	2	0	0	0	0	0	0	1	0	0	1	5	4	1	1	2	7
Type 15:	35	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	11	23	1	0	0	0
Type 16:	70	0	0	0	1	0	0	2	0	0	0	0	3	0	0	0	0	0	37	22	3	0	0	2
Type 17:	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8	0	0	0	0	0
Type 18:	66	0	0	0	0	1	7	35	0	0	2	9	0	4	0	0	0	0	0	0	0	0	0	8
Type 19:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type 20:	3	0	0	0	0	0	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type 21:	34	0	0	0	0	0	0	34	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Type 22:	244	0	1	1	13	19	32	10	0	1	0	0	0	1	2	1	0	0	0	2	0	1	0	160
TOTAL	1292	7	124	13	27	90	88	171	35	31	2	9	3	10	18	181	2	1	89	70	5	8	7	301

circuits are not included. In addition to lot specific defects, some expected similar defect types patterns are discernible. In particular: types 12 and 13 of defects Ssp and Dsp, and types 14 through 16 of defects Dop and Don. In the latter case, a process change was introduced between lot 10433 and 11851 which accounts for the reduction in defect density. Also, defect types 4 and 21 were more frequent for lot 11851.

From the point of view of the algorithm only 20–35% of the defects had unknown signatures. Meaning these defects were too large or included shorts between more than 2 layers. All other faults were readily identified and located with the algorithm. Only 15% of the faults could not be identified with the algorithm and could not be located with optical microscope (unknown signature and unknown physical type).

An interesting avenue would be to use fuzzy logic to locate and identify the faults. The signatures obtained by simulations could be used for learning. Such a machine would probably be a very efficient and very fast mean for determining the position and nature of faults in the case where there is more than one defect per circuit.

Conclusion

We have developed an integrated circuit (Yieldchip) which enables process induced faults to be identified and located electrically. Simulations showed that electrical fault identification was unique. Fabrication and testing of the circuit proved that it works in accordance with simulation results. At the moment we are using this device to perform defect characterization of a production line. In the future we intend to experiment the use of the yieldchip for process reliability characterization.

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