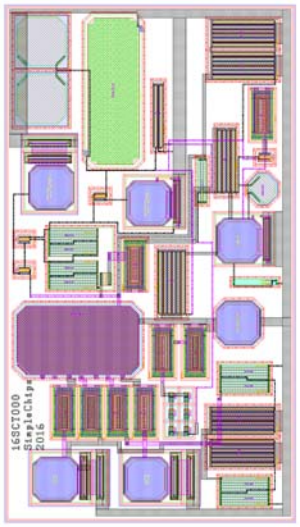
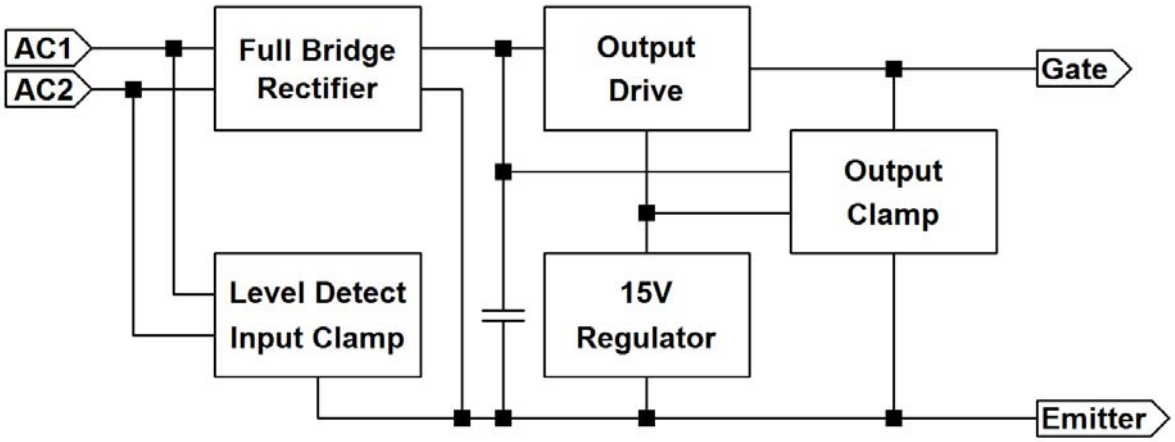
- Maximum Voltage. . . 30 V;
- Transformer Drive provides HV isolation;
- No other external components required;
- Fast IGBT Turn-On & Turn-Off Times.



Description

The 16SCT000 is an IGBT/MOSFET gate driver (15V nominal Vg) chip to control the conduction state of a high-side switch from the secondary of a small high-voltage isolation transformer. The 16SCT000 will drive the gate of the HV switch above the emitter/source while the secondary winding of the transformer drives the complementary input signals. Upon cessation of the input drive signals, the 16SCT000 quickly clamps the gate to the emitter/souce terminal to ensure fast turns off.

Block diagram



Concept of operation

In normal operation an square wave alternating signal is applied between AC1 and AC2. This signal is rectified by the Full Bridge and the resulting voltage is stored on the integrated capacitor. The rectified DC voltage is then applied to the 15V Regulator and fed to the Gate via the Output Drive circuit. This voltage saturates on the IGBT/MOSFET into a low resistance conduction state.

After the AC drive signal is removed, the voltage stored on the integrated capacitor falls. When it falls below the voltage on the Gate, the Output Clamp shunts the Gate and various internal nodes, rapidly turning off the IGBT/MOSFET. The Clamp Circuit has a time constant of several tens of microseconds, ensuring that the Gate and internal nodes are clamped solidly for that duration. The Output Clamp circuit also acts to prevent false triggering when voltages change rapidly.

Absolute maximum ratings

Input Voltage (AC1 - AC2) . . . . . +/-30 V
Operating temperature . . . . . 0 C to 80 C
Storage temperature. . . . . -65 C to 125 C

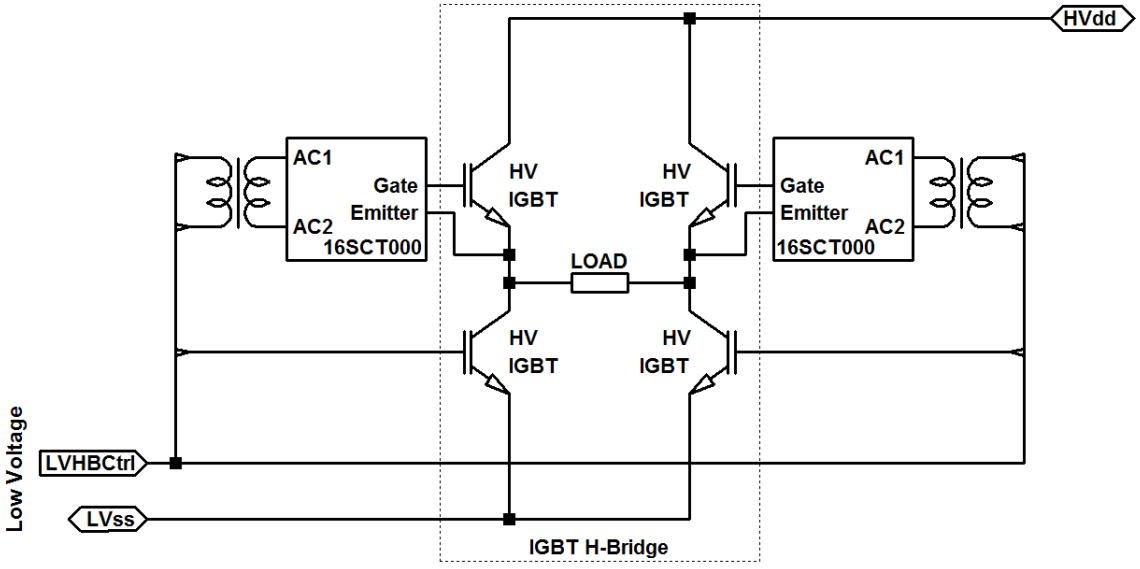
Recommended operating conditions

PARAMETER	MIN	MAX	UNIT
Operating temperature	0	80	^{o}C
Operating voltage, AC1 - AC2, peak, complementary phase		25	V_{ac}
Operating frequency, AC1 - AC2	0.40	5.0	MHz
Continuous power dissipation (AC1 - AC2 drive signal applied)	25	300	mW

Pin definitions

SYMBOL	DESCRIPTION
AC1	AC input drive signal
AC2	AC input drive signal
Gate	Gate terminal of the high-side IGBT/MOSFET
Emitter/ Source	Emitter/Source terminal of the high-side IGBT/MOSFET

Typical application



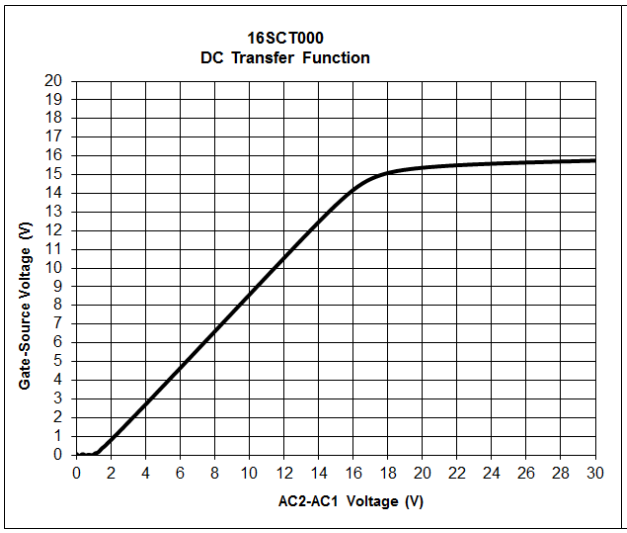
Static electrical characteristics($37^oC \pm 2^oC$ unless specified)

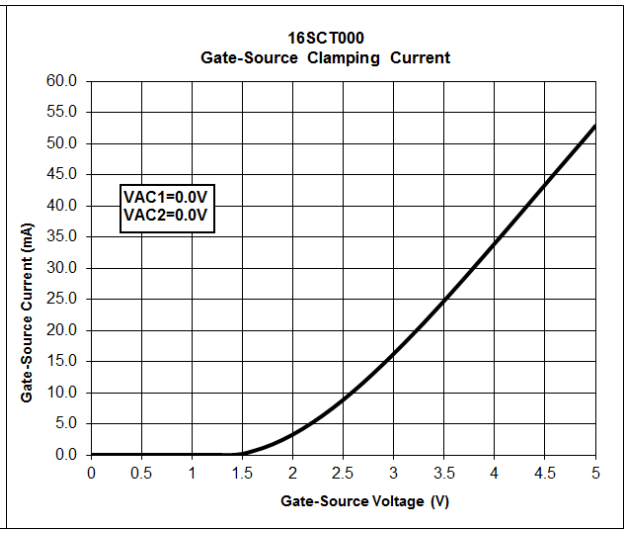
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ge15NL}	Output Voltage, No Load	$V_{AC1/2}$=15V, $V_{AC2/1}$=0V	12.52	13.38	14.05	V
V_{ge25NL}	Output Voltage, No Load	$V_{AC1/2}$=25V, $V_{AC2/1}$=0V	14.55	15.44	16.16	V
V_{ge15}	Output Voltage, -2mA Load	$V_{AC1/2}$=15V, $V_{AC2/1}$=0V	11.75	12.53	13.18	V
V_{ge25}	Output Voltage, -2mA Load	$V_{AC1/2}$=25V, $V_{AC2/1}$=0V	14.00	14.88	15.63	V
V_{geCL}	Gate Clamping V, Low Current	$V_{AC1/2}$=0V, I_{ge}=0.5mA	1.18	1.57	1.94	V
$I_{ge3.5}$	Gate Clamping Current	$V_{AC1/2}$=0V, V_{ge}=3.5	13.0	26.0	40.0	mA
R_{ge}	Gate-Emitter/Source Resistance	V_{ge}=0.4V	183	440	707	kΩ
$R_{AC1/2L}$	Input Resistance; Low Voltage	$V_{AC1/2}$=0.25V, $V_{AC2/1}$=0V	64.0	81.1	95.9	kΩ
$R_{AC1/2M}$	Input Resistance; Med Voltage	$V_{AC1/2}$=[4-8]V, $V_{AC2/1}$=0V	37.3	47.2	57.9	kΩ
$R_{AC1/2H}$	Input Resistance; Above 18V	$V_{AC1/2}$=[30-18]V, $V_{AC2/1}$=0V	11.1	16.4	19.3	kΩ
$Delta_R$	Resistance Matching Above 18V	$V_{AC1/2}$=[30-18]	-10	0	+10	%

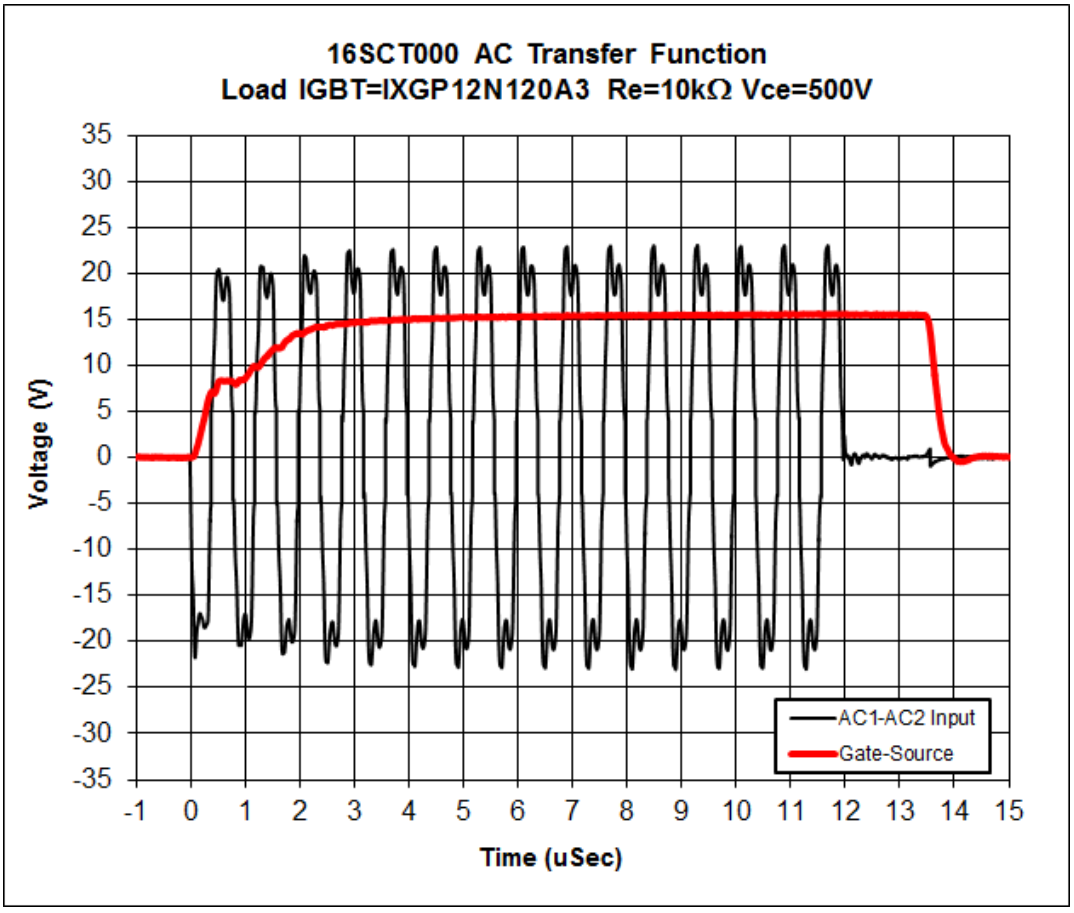
Dynamic electrical characteristics ($37^oC \pm 2^oC$)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{cd1.0}$	Gate Charge Delay 1.0nF	C_{Load}=1.0nF, 0 to 20V pulse on AC1 - AC2, $t_{cd1.0}$ measured at V_{ge}=2V		65		nS
$t_{ct1.0}$	Gate Charge Time 1.0nF	C_{Load}=1.0nF, 0 to 20V pulse on AC1 - AC2, $t_{ct1.0}$ measured from V_{ge}=2V to 12V		325		nS
$t_{dd1.0}$	Gate Discharge Delay 1.0nF	C_{Load}=1.0nF, 20 to 0V pulse on AC1 - AC2, t_0 when $V_{AC1/2}$=15V, $t_{dd1.0}$ when V_{ge}=12V	0.80	1.33	2.50	µS
$t_{dt1.0}$	Gate Discharge Time 1.0nF	C_{Load} = 1.0nF, 20 to 0V pulse on AC1 - AC2, t_0 when $V_{AC1/2}$=12V, $t_{dt3.3}$ when V_{ge}=2V	0.05	0.10	0.20	µS
$t_{cd3.3}$	Gate Charge Delay 3.3nF	C_{Load}=3.3nF, 0 to 20V pulse on AC1 - AC2, $t_{cd3.3}$ measured at V_{ge}=2V		150		nS
$t_{ct3.3}$	Gate Charge Time 3.3nF	C_{Load}=3.3nF, 0 to 20V pulse on AC1 - AC2, $t_{ct3.3}$ measured from V_{ge}=2V to 12V		1000		nS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{dd3.3}$	Gate Discharge Delay 3.3nF	C_{Load}=3.3nF, 20 to 0V pulse on AC1 - AC2, t_0 when $V_{AC1/2}$=15V, $t_{dd3.3}$ when V_{ge}=12V	0.8	1.33	2.5	µS
$t_{dt3.3}$	Gate Discharge Time 3.3nF	C_{Load} = 3.3nF, 20 to 0V pulse on AC1 - AC2, t_0 when $V_{AC1/2}$=12V, $t_{dt3.3}$ when V_{ge}=2V	0.145	0.25	0.338	µS

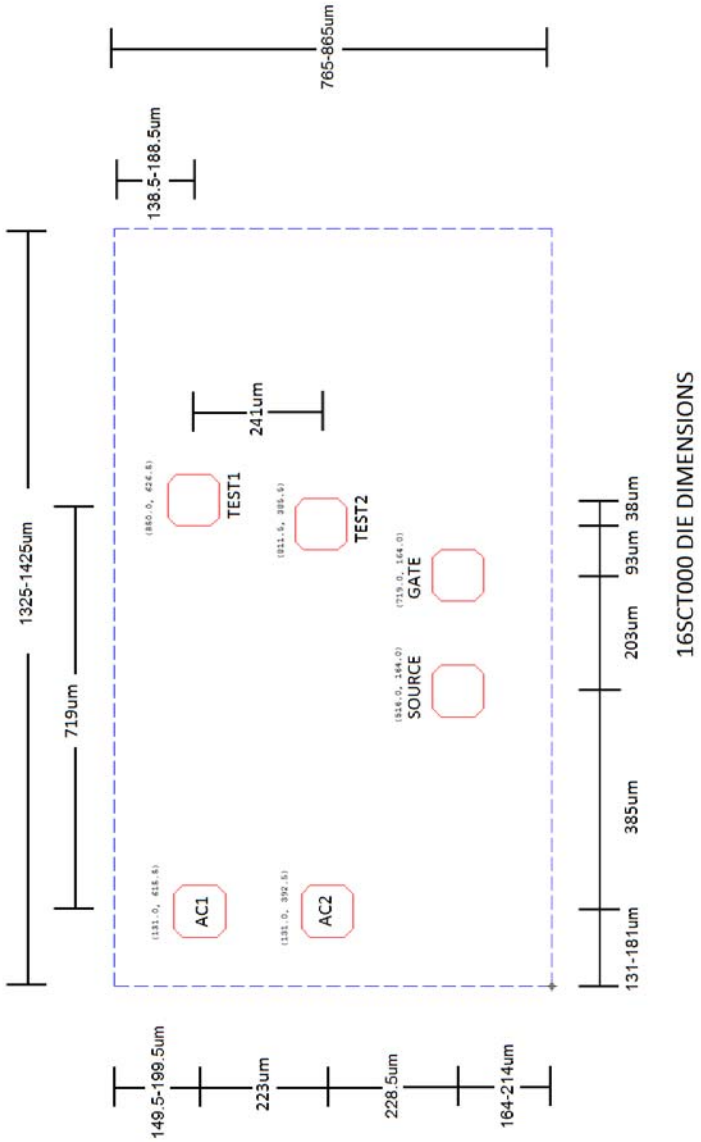






Die Dimensions

PARAMETER		MIN	TYP	MAX	UNIT
Y_{SIZE}	Long Side Dimensions	1325	1375	1425	µm
X_{SIZE}	Short Side Dimensions	765	815	865	µm
Z_{SIZE}	Die Thickness	260	285	310	µm



Visual inspection

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
100% Visual Inspection per MIL STD 883H Method 2010 Condition B.	ALL	100%	n/a	n/a

Product qualification tests

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
Static burn-in 504hrs @ V_{HV}=1000V; MIL STD 883 method 1015	3	22	0	n/a
Physical dimensions	3	11	0	n/a
Wire Bond Evaluation (Gold Ball Bond) per MIL STD 883 method 2011	3	20	1	n/a

Lot acceptance tests

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
Static burn-in 168hrs @ V_{HV}=1000V; MIL STD 883 method 1015	each	22	0	n/a
Physical dimensions	each	11	0	n/a
Wire Bond Evaluation (Gold Ball Bond) per MIL STD 883 method 2011	each	20	1	n/a

Product qualification tests are performed on 3 lots while a Lot Acceptance Test (LAT) is performed on each “diffusion lot”. LAT is considered complete if the lot was used for product qualification.

All samples used for qualification and LAT burn-in test are assembled in a open cavity ceramic DIL package with a dielectric silicone gel filling the cavity. Tthe chip is mounted to provide isolation between the wirebonds and the substrate and to eliminate surface conduction and polarization as possible means of unwanted failure.

Application notes

To make best use of the 16SCT000, the chip should be molded before high voltage is applied to it. This can either be done with a standard mold compound or with silicone gel. Care should be taken when selecting a encapsulant to ensure proper dielectric strength and resistance. We recommend that the dielectric strength of the dielectric used be greater than 10kV/mm at a thickness of 50um.

Care should also be taken to properly isolate the chips substrate which is biased at about half V_{HV}. In no circumstance should the chip be mounted over layers providing less than 1kV of dielectric isolation. It is also strongly recommended to use non-conducting epoxy for attaching the chip.

Ball bonding should be used for attaching conductors to the chip's pad. Wedge bonding is not recommended because of the shorter distance between the wirebond and the chip's edge, increasing the risk of arcing. When using ball bonding the wire should extend vertically for at least 150um before going horizontal toward the substrate or package pad.