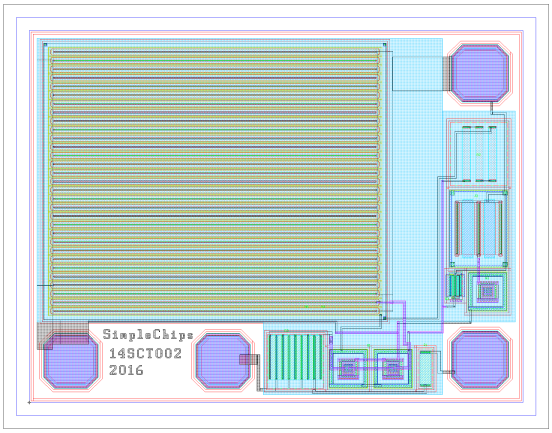
14SCT002
OPTO-COUPLER or SSR LED DRIVER

- **Metal Shield to prevent LED interaction.**
- **Nominal Current 14mA**
- **Resistor programmable current**
- **-55C to +125C operation**
- **Small die size at 1050um X 815um**
- **Breakdown voltage > 50V**
- **OFF leakage < +/-100uA**

DIE

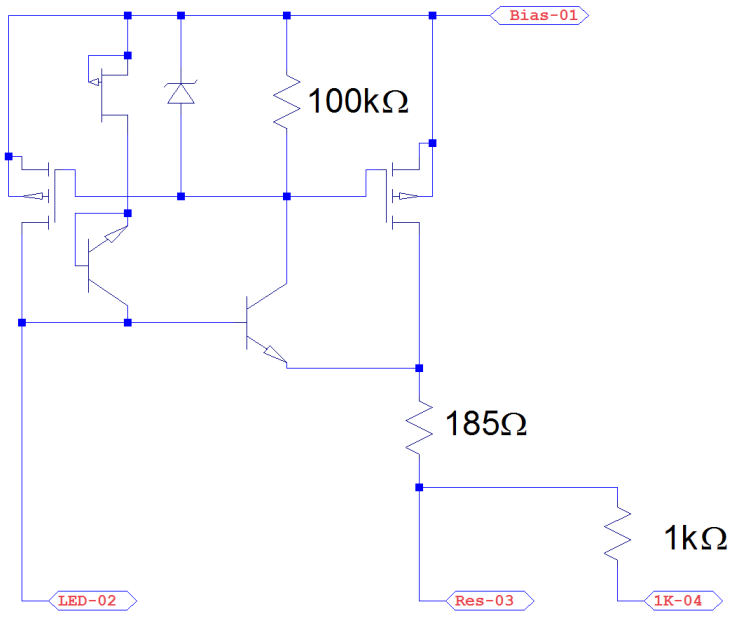
(TOP VIEW)



Description

This device is a resistor programmable current limiter for use in opto-coupler or solid-state relays were a premium is placed on product quality and performance. Nominally set for 14mA using industry standard 2kΩ resistor setting resistor the 14SCT002 delivers steady performance across the entire extended temperature range of -55C to 125C.

Equivalent circuit:



Absolute maximum rating

Input Voltage (V_{HV} - V_{SS}) . . . . . +/-50 V
Operating temperature . . . . . -55 C to 125 C
Storage temperature. . . . . -65 C to 150 C

Electrical charateristics at room temperature (25C +/- 2C) (100% tested)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ID_{LV2}	Low Voltage LED Current	V_{Bias}=4.0V; V_R=2.60V; R=2.0k	11.3	13.1	14.9	mA
ID_{HV2}	High Voltage LED Current	V_{Bias}=32.0V; V_R=2.60V; R=2.0k	11.2	12.9	14.7	mA
ID_{LV8}	Low Voltage LED Current 2	V_{Bias}=5.0V; V_R=2.70V; R=0.80k	28.0	33.0	39.2	mA
$I_{LV2.0}$	Low Voltage Bias Current	V_{Bias}=4.0V; V_R=2.60V; R=2.0k	12.1	14.0	15.9	mA
$I_{HV2.0}$	High Voltage Bias Current	V_{Bias}=32.0V; V_R=2.60V; R=2.0k	11.9	13.8	15.7	mA
$I_{LV0.8}$	Low Voltage Bias Current 2	V_{Bias}=5.0V; V_R=2.70V; R=0.80k	29.9	35.4	42.0	mA
R_{Set}	Set Resistor	V=1.0V	0.75	1.10	1.35	kΩ
I_{R32}	Leakage Current at -32V	V_{Bias}=-32.0V; V_R=0.00V; R=0.0k	-100	-1.0	0	nA
I_{T+50}	Leakage Current at +50V	V_{Bias}=50.0V; V_R=0.00V; R=0.0k	10	31.0	100	µA
I_{T-50}	Leakage Current at -50V	V_{Bias}=-50.0V; V_R=0.00V; R=0.0k	-100	-1.3	0	nA
$I_{S3.8}$	Start-up Current at 3.8V	V_{Bias}=3.8V; V_R=0.00V; R=0.0k	5.0	18	100	µA
I_{S32}	Start-up Current at 32V	V_{Bias}=-32.0V; V_R=0.00V; R=0.0k	10	27.0	100	µA

Electrical charateristics at COLD temperature (-55C +/- 2C) (Sample tested)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ID_{CLV2}	Low Voltage LED Current	V_{Bias}=4.0V; V_R=2.25V; R=2.0k	11.6	13.4	15.1	mA
ID_{CHV2}	High Voltage LED Current	V_{Bias}=32.0V; V_R=2.25V; R=2.0k	11.4	13.3	15.0	mA
ID_{CLV8}	Low Voltage LED Current 2	V_{Bias}=5.0V; V_R=2.45V; R=0.80k	28.0	34.8	39.2	mA
$I_{CLV2.0}$	Low Voltage Bias Current	V_{Bias}=4.0V; V_R=2.25V; R=2.0k	12.5	14.4	16.2	mA
$I_{CHV2.0}$	High Voltage Bias Current	V_{Bias}=32.0V; V_R=2.25V; R=2.0k	12.2	14.3	16.1	mA
$I_{CLV0.8}$	Low Voltage Bias Current 2	V_{Bias}=5.0V; V_R=2.45V; R=0.80k	30.0	37.3	42.0	mA
I_{CR32}	Leakage Current at -32V	V_{Bias}=-32.0V; V_R=0.00V; R=0.0k	-100	-20	0	nA
I_{CT+50}	Leakage Current at +50V	V_{Bias}=50.0V; V_R=0.00V; R=0.0k	10	37	100	µA
I_{CT-50}	Leakage Current at -50V	V_{Bias}=-50.0V; V_R=0.00V; R=0.0k	-100	-27	1	nA
$I_{CS3.8}$	Start-up Current at 3.8V	V_{Bias}=3.8V; V_R=0.00V; R=0.0k	5	23	100	µA
I_{CS32}	Start-up Current at 32V	V_{Bias}=-32.0V; V_R=0.00V; R=0.0k	10	32	100	µA

Electrical charateristics at HOT temperature (125C +/- 2C) (Sample tested)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ID_{HLV2}	Low Voltage LED Current	V_{Bias}=4.0V; V_R=2.85V; R=2.0k	11.8	13.7	15.6	mA
ID_{HHV2}	High Voltage LED Current	V_{Bias}=32.0V; V_R=2.85V; R=2.0k	11.7	13.6	15.5	mA
ID_{HLV8}	Low Voltage LED Current	V_{Bias}=5.0V; V_R=3.10V; R=0.80k	28.0	33.5	39.2	mA
$I_{HLV2.0}$	Low Voltage Bias Current	V_{Bias}=4.0V; V_R=2.85V; R=2.0k	12.7	14.7	16.7	mA
$I_{HHV2.0}$	High Voltage Bias Current	V_{Bias}=32.0V; V_R=2.85V; R=2.0k	12.6	14.6	16.6	mA
$I_{HLV0.8}$	Low Voltage Bias Current	V_{Bias}=5.0V; V_R=3.10V; R=0.80k	30.0	35.9	42.0	mA
I_{HR32}	Leakage Current at -32V	V_{Bias}=-32.0V; V_R=0.00V; R=0.0k	-20	-1.5	0	µA
I_{HT+50}	Leakage Current at +50V	V_{Bias}=50.0V; V_R=0.00V; R=0.0k	10	34.0	100	µA
I_{HT-50}	Leakage Current at -50V	V_{Bias}=-50.0V; V_R=0.00V; R=0.0k	-20	-1.8	0	µA
$I_{HS3.8}$	Start-up Current at 3.8V	V_{Bias}=3.8V; V_R=0.00V; R=0.0k	5	19.0	100	µA
I_{HS32}	Start-up Current at 32V	V_{Bias}=-32.0V; V_R=0.00V; R=0.0k	10	28.0	100	µA

Die dimensions

PARAMETER		MIN	TYP	MAX	UNIT
Y_{SIZE}	Long Side Dimensions	1000	1050	1100	µm
X_{SIZE}	Short Side Dimensions	765	815	865	µm
Z_{SIZE}	Die Thickness	260	285	310	µm

Product qualification tests

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
Static burn-in 1000hrs @ V_{BIAS}=32V; MIL STD 883 method 1015	3	22	0	n/a
Physical dimensions	3	11	0	n/a
Wire Bond Evaluation (Gold Ball Bond) per MIL STD 883 method 2011	3	20	1	n/a
COLD temperature electrical test	each	22	0	n/a
HOT temperature electrical test	each	22	0	n/a

Visual inspection

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
100% Visual Inspection per MIL STD 883H Method 2010 Condition S.	ALL	100%	n/a	n/a

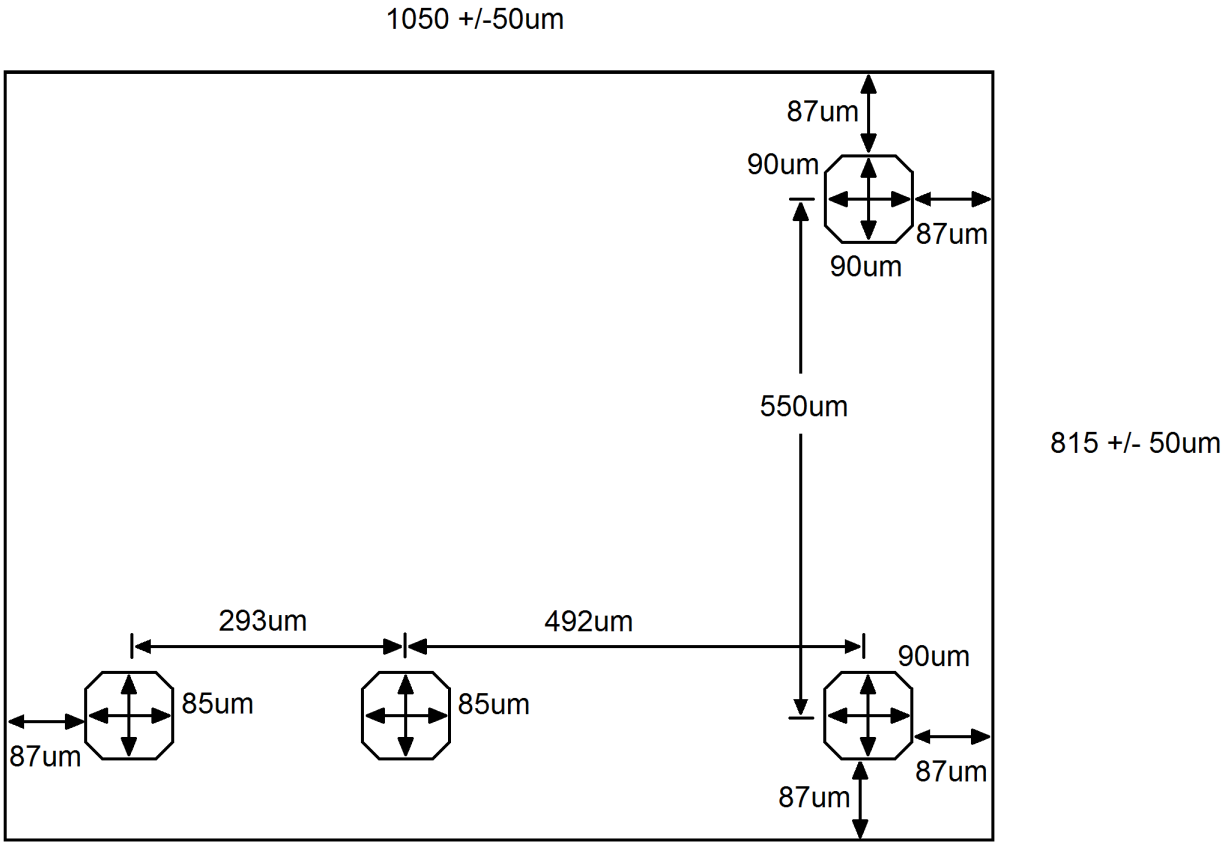
Lot acceptance tests

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
Static burn-in 125C; 168hrs; V_{BIAS}=32V; Vr=2.25V; R=2000 Ohm MIL STD 883 method 1015	each	22	0	n/a
Physical dimensions	each	11	0	n/a
Wire Bond Evaluation (Gold Ball Bond) per MIL STD 883 method 2011	each	20	1	n/a
COLD temperature electrical test	each	22	0	n/a
HOT temperature electrical test	each	22	0	n/a

Product qualification tests are done on 3 batches only while lot acceptance test are performed on each “diffusion lot”. Lot acceptance tests (LAT) are considered done if the lot in question was used for product qualification.

All samples used for qualification and LAT burn-in test are assembled in a open cavity ceramic DIL package with a dielectric silicone gel filling the cavity where the chip is mounted to provide isolation between the wirebonds and the substrate and to eliminate surface conduction and polarization as possible means of unwanted failure.

Die dimensions



Pin-Out